UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,125	12/31/2003	James A. Kirchgessner	0129185	9774

7590 12/02/2005

Kenneth A. Nelson
Bryan Cave LLP
Suite 2200
Two North Central Avenue
Phoenix, AZ 85004-4406

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,125	KIRCHGESSNER, JAMES A.	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-19* is/are allowed.

6)☒ Claim(s) *1,2,9,10,20,22 and 23* is/are rejected.

7)☒ Claim(s) *3-8 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The Applicant argues that the 35 U.S.C. 102(b) rejection as being anticipated by U.S. Patent No. 6,472,753 Kondo et al. does not teach the buried layer to be underneath a portion of a trench. The examiner has considered the Applicant's arguments, but finds them to be non-persuasive. The examiner does agree that the BOX element #2 is not underneath the trench #7, but the 35 U.S.C. 102(b) rejection as being anticipated by U.S. Patent No. 6,472,753 Kondo et al., filed on 6/16/05, never used elements #2 and #7 in the rejection. The Applicant's arguments never discussed the elements, (#4 and #6), that were used to reject the claims, but instead used elements selected by the Applicant, (#2 and #7). The rejection filed on 6/16/05 used the element #4 as the buried layer in the substrate, which is illustrated in Figures 20a-e & 21a-c and in Col. 10 Lines 51-52. The rejection also used the element #6, which is best seen in Figure 20e as the trench. Figure 20b details the step where trench #6 was formed in the substrate and in Figure 20a details how layer #5 is the upper surface of the substrate #1, hence the trench #6 is formed in the substrate #1. Figure 20e teaches the limitation where the buried layer #4 is underneath the trench #6, hence the rejection under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,472,753 Kondo et al. for claims 1, 2, 9, and 10 stands as is.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,472,753 Kondo et al.

2. Referring to claim 1, a method of manufacturing a semiconductor component, the method comprising: providing a semiconductor substrate, (Figures 20a-e & 21a-c #1 and Col. 10 Lines 50-51), having a surface and a first conductivity type; forming a trench, (Figures 20a-e & 21a-c area of #6), in the surface of the semiconductor substrate, (Figures 20a-e & 21a-c #1), to define a plurality of active areas, (Figures 20a-e & 21a-c area of #3 & 5), separated from each other by the trench, (Figures 20a-e & 21a-c area of #6); forming a buried layer, (Figures 20a-e & 21a-c #4), in the semiconductor substrate, (Figures 20a-e & 21a-c #1), underneath a portion of the trench, (Figures 20a-e & 21a-c area of #6), wherein the buried layer, (Figures 20a-e & 21a-c #4 Col. 10 Lines 51-52), has a second conductivity type and is at least partially contiguous with the trench, (Figures 20a-e & 21a-c area of #6); after forming the buried layer, (Figures 20a-e & 21a-c #4), depositing an electrically insulating material in the trench, (Figures 20a-e & 21a-c #6); forming a collector region, (Figures 20a-e & 21a-c #5 Col. 10 Line 52), having the second conductivity type in one of the plurality of active areas, (Figures 20a-e & 21a-c area #5); forming

a base structure having the first conductivity type, (Figures 20a-e & 21a-c #182 Col. 14 Lines 55-56), over the one of the plurality of active areas, (Figures 20a-e & 21a-c area of #5); and forming an emitter region, (Figures 20a-e & 21a-c #21 Col. 10 Line 58), having the second conductivity type over the one of the plurality of active areas, (Figures 20a-e & 21a-c area of #5), wherein; the collector region, (Figures 20a-e & 21a-c #5), forms a contact to the buried layer, (Figures 20a-e & 21a-c #4).

3. Referring to claim 2, a method wherein; the collector region, (Figures 20a-e & 21a-c #5 Col. 10 Line 52 Low doped*), has a first resistivity; the buried layer, (Figures 20a-e & 21a-c #4 Col. 10 Lines 51-52), has a second resistivity; and the first resistivity is greater than the second resistivity.

4. Referring to claim 9, a method, wherein; manufacturing the semiconductor component comprises: manufacturing the one of the plurality of active areas, (Figures 20a-e & 21a-c #5), to be symmetric, (partially symmetric up to the point where the left side insulative trench is buried deeper into the substrate), about a vertical line drawn through a middle of the emitter region, (Figures 20a-e & 21a-c #21).

5. Referring to claim 10, a semiconductor component, (Figure 21c), formed by the method of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,472,753 Kondo et al.

6. Referring to claim 20, a method of manufacturing a semiconductor component, the method comprising: providing a semiconductor substrate, (Figures 20a-e & 21a-c #1 and Col. 10 Lines 50-51), having a surface and a first conductivity type, where the semiconductor substrate, (Figures 20a-e & 21a-c #1), comprises a plurality of bipolar semiconductor regions, (Figures 20a-e & 21a-c area of #5 and see ** below), and a plurality of CMOS regions, (Figures 20a-e & 21a-c area of #9 and see ** below); forming a trench, (Figures 20a-e & 21a-c area of #6) in the surface of the semiconductor substrate, (Figures 20a-e & 21a-c #1), in the plurality of bipolar semiconductor regions, (Figures 20a-e & 21a-c area of #5 and see ** below), and in the plurality of CMOS regions, (Figures 20a-e & 21a-c area of #9 and see ** below), to define a plurality of active areas, (Figures 20a-e & 21a-c #3 & 5), separated from each other by the trench, (Figures 20a-e & 21a-c area of #6); forming a buried layer, (Figures 20a-e & 21a-c #4), in the semiconductor substrate, (Figures 20a-e & 21a-c #1), underneath a portion of the trench, (Figures 20a-e & 21a-c area of #6), in the plurality of bipolar semiconductor regions, (Figures 20a-e & 21a-c area of #5 and see ** below), where the buried layer has a second conductivity type, (Figures 20a-e & 21a-c #4 Col. 10 Lines 51-52), and is at least partially contiguous with the

trench, (Figures 20a-e & 21a-c area of #6); after forming the buried layer, (Figures 20a-e & 21a-c #4 Col. 10 Lines 51-52), depositing an electrically insulating material in the trench, (Figures 20a-e & 21a-c #6); forming a collector region having the second conductivity type, (Figures 20a-e & 21a-c #5 Col. 10 Line 52 *Low doped*) in each one of the plurality of bipolar semiconductor regions, (Figures 20a-e & 21a-c area of #5 and see ** below); forming a base structure having the first conductivity type, (Figures 20a-e & 21a-c #182 Col. 14 Lines 55-56), over each one of the plurality of bipolar semiconductor regions, (Figures 20a-e & 21a-c area of #5 and see ** below); forming an emitter having the second conductivity type, (Figures 20a-e & 21a-c #21 Col. 10 Line 58), over each one of the plurality of bipolar semiconductor regions, (Figures 20a-e & 21a-c area of #5 and see ** below); forming source/drain regions, (Figures 20a-e & 21a-c #12), over each one of the plurality of CMOS regions, (Figures 20a-e & 21a-c area of #9 and see ** below); and forming a gate region, (Figures 20a-e & 21a-c #9), over each one of the plurality of CMOS regions, (Figures 20a-e & 21a-c area of #9 and see ** below), wherein: the collector region, (Figures 20a-e & 21a-c #5), forms a contact to the buried layer, (Figures 20a-e & 21a-c #4).

** Kondo et al. discloses the claimed invention except for the plurality of bipolar regions and plurality of cmos regions. It would have been obvious to one having skill in the art at the time the invention was made to have a plurality of bipolar and cmos regions, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. vs Bomis Co. 193USPQ8

7. Referring to claim 22, a method, wherein: the collector region has a first resistivity, (Figures 20a-e & 21a-c #5 Col. 10 Line 52 *Low doped*); the buried layer has a second

resistivity, (Figures 20a-e & 21a-c #4 Col. 10 Lines 51-52); and the first resistivity is greater than the second resistivity.

8. A semiconductor component formed by the method of claim 20, (Figure 21c).

Allowable Subject Matter

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art teaches a first conductivity semiconductor substrate having regions therein that are of the first and second conductivity, wherein a trench is formed in the substrate which defines a plurality of active regions, wherein a mask is formed to form buried regions of the second conductivity type in the substrate underneath the trench and where the trenches are filled with an insulative material, a collector region formed having the second conductivity, an emitter formed having the second conductivity, wherein the collector contacts the buried layer. The prior art does not teach the above teachings in combination with the trenches having spacers formed therein and where the buried layer is self aligned with the trench and spacers, which are later removed before depositing the insulative material. This combination has been found to be non-obvious thus novel.

10. Claims 11-19 are allowed.

11. Claims 3-8 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
11/15/05

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800